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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,254	09/18/2003	Ling-Wuu Yang	9676-US-PA	2253

31561 7590 09/24/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
KEBEDE, BROOK	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,254	YANG ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because of the following reasons:

Figs. 1A – 1G include sectional views I-I'. However, "the ends of the broken line" should be designated by Arabic numerals corresponding to the view number of the sectional view. See 37 C.F.R § 1.84(h)(3). Additionally, applicant is requested to accordingly amend the specification. For example, see specification in page 4, paragraph [0014], line 4 and throughout.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "patterning the strip structure to **form a control gate structure**, in which the **patterned conductive layer is further patterned into a floating gate,**" as claimed in claim 1, lines 8-10, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the

drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 2, and 12 are objected to because of the following informalities:

Claim 2 recites the limitation "floating gate **structures**" in lines 4, 5, and 7. However, the recited claim lacks proper antecedent basis. Appropriate correction is required.

Claim 12 recites the limitation "floating **gates**" in line 4. However, the recited claim lacks proper antecedent basis. Appropriate correction is required.

4. Claim 11 objected to under 37 CFR 1.75(c), for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 11 recites the limitation "forming a buried drain region in the substrate between the floating gates" in lines 4-5 and "performing an ion implantation step to form a buried drain region in the substrate between the floating gates" in lines 6-7. However, the recitation in lines 4-5 is already encompass the formation of drain region which inherently requires ion implantation.

Therefore, the limitation "performing an ion implantation step to form a buried drain region in the substrate between the floating gates" in lines 6-7 does not further the previously claimed claim limitation in lines 4-5.

5. Claim 18 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the

claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 18 recites the limitation "The method according to **Claim 18**, further comprising using wet etching to remove the mask layer" in lines 1-2. However, the dependency of claim 18 to itself is improper.

For examination purpose, claim 18 is treated as being depending upon claim 11. However, upon amendment, if an alternative interpretation of claim dependency requires a change in the rejection, the new rejection may properly **made final**.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "patterning the strip structure to form a control gate structure, in which the patterned conductive layer is further patterned into a floating gate" in lines 8-10. However, the recited claim lacks clarity because of the following reasons:

The strip structure, as depicted in Fig. 2B, consisting of a tunnel oxide layer pattern **102a**; a conductive layer pattern **104a**; and a mask layer pattern (i.e., Si_3N_4 layer) **106a**. In addition, Fig. 2C depicts the patterned layers (**102b 104b 106b**) and floating gate structure. However it is not clear that how the control gate can be formed by further pattering of layers **102a 104a 106a**.

In addition, as recited in claim 1 (as shown on Fig. 2G), the control gate **120** formed on the gate dielectric layer **114**, as independent from the conducive layer (floating gate) 104b.

It is not clear how pattering of the conductive pattern **104a** forms the control gate and the formation of the control gate, as claimed in claim 1, is contradictory and it creates a great deal of confusion in terms the claim's scope and meaning. Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2-10 are also rejected as being directly and/or indirectly dependent of the rejected independent base claim

Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

In light of the rejection 35 U.S.C. § 112 second Paragraph *supra*, the following 35 U.S.C. 102 rejection is based on prior art which reads on the interpretation the claim language of the instant application as best as understood by the Examiner.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4, 6-9, 11-14, and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (US/6,413,818).

Re claim 1, Huang et al. disclose a method of fabricating a flash memory, comprising: sequentially forming a tunneling dielectric layer (303), a first conductive layer (304) and a mask layer (306) on a substrate (300) (see Fig. 3A); patterning the tunneling dielectric layer (303), the first conductive layer (304) and the mask layer (306) into a strip structure (see Fig. 3B); performing an ion implantation step to form a buried drain region (314 315) in the substrate (300) between the strips (see Fig. 3B); thereby forming the floating gate pattern (304); forming an insulation (i.e., an isolation oxide) layer (326) on a sidewall of the floating gate structure (304 324) (see Fig. 3C) ; removing the patterned mask layer (306) (see Fig. 3D); forming a second conductive layer (324) over the first conducive layer pattern (304) and the insulation layer (326); patterning the second conductive layer (324) to form the floating gate composed of the first conductive layer (304) and second conducive layer (324) (see Fig. 3F); etching back the insulation layer (326) to form the insulation layer having a top surface lower than a top surface of the floating gate such that a part of a sidewall of the floating gate is exposed (see Fig. 3G); forming a gate dielectric layer (316) on the top surface and the exposed sidewall of the floating gate; and forming a control gate (360) on the gate dielectric layer (316) (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 2, as applied to claim 1 above, Huang et al. disclose all the claimed limitation including the limitation wherein the step of forming the insulation layer (326) further comprises: forming an insulation layer (326) on the substrate (300); to cover the floating gate structures (304) and to fill space between the floating gate structures (304); removing a part of the insulation layer that covers the floating gate structures to expose the patterned mask layer (306) (see Fig. 3C); and removing a part of the remaining insulation layer (326) until the top surface of

the insulation layer is between a top surface and a bottom surface of the floating gate (see Fig. 3G) (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 3, as applied to claim 2 above, Huang et al. disclose all the claimed limitation including the limitation forming the insulation layer with silicon oxide (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 4, as applied to claim 2 above, Huang et al. disclose all the claimed limitation including the limitation using high-density plasma chemical vapor deposition (see Col. 7, lines 57-59) for forming the insulation layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 6, as applied to claim 2 above, Huang et al. disclose all the claimed limitation including the limitation using CMP (see Col. 7, lines 42-46) to remove part of the insulation layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 7, as applied to claim 2 above, Huang et al. disclose all the claimed limitation including the limitation using etch back (see Fig. 3G) to remove the remaining insulation layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 8, as applied to claim 1 above, Huang et al. disclose all the claimed limitation including the limitation forming the mask layer with silicon oxide or silicon nitride (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 9, as applied to claim 1 above, Huang et al. disclose all the claimed limitation including the limitation using wet etching to remove the mask layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 11, Huang et al. a method of fabricating a flash memory, comprising: forming a tunneling dielectric layer (303) and a floating gate (304) on a substrate (300); forming a buried

drain (315 316) region in the substrate (300) between the floating gates by ion implantation step in the substrate between the floating gates (see Fig. 3B); forming an insulation layer on a sidewall of the floating gate (326), the insulation layer having a top surface level between a top surface and a bottom surface of the floating gate (304 324); forming a gate dielectric layer (316) on the top surface and the exposed sidewall of the floating gate; and forming a control gate (360) on the gate dielectric layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 12, as applied to claim 11 above, Huang et al. disclose all the claimed limitation including the limitation wherein the step of forming the insulation layer further comprises: forming an insulation layer (326) on the substrate (300); to cover the floating gate structures (304) and to fill space between the floating gate structures (304); removing a part of the insulation layer that covers the floating gate structures to expose the patterned mask layer (306) (see Fig. 3C); and removing a part of the remaining insulation layer (326) until the top surface of the insulation layer is between a top surface and a bottom surface of the floating gate (see Fig. 3G) (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 13, as applied to claim 12 above, Huang et al. disclose all the claimed limitation including the limitation forming the insulation layer with silicon oxide (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 14, as applied to claim 13 above, Huang et al. disclose all the claimed limitation including the limitation using high-density plasma chemical vapor deposition (see Col. 7, lines 57-59) for forming the insulation layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 16, as applied to claim 12 above, Huang et al. disclose all the claimed limitation including the limitation using CMP (see Col. 7, lines 42-46) to remove part of the insulation layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 17, as applied to claim 1 above, Huang et al. disclose all the claimed limitation including the limitation forming a mask on the floating gate when the part of the insulation layer formed subsequently is removed by chemical mechanical polishing; and a step of removing the mask layer before forming the gate dielectric layer, wherein the mask layer is made of a material different from that of the insulation layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 18, as applied to claim 11 above, Huang et al. disclose all the claimed limitation including the limitation using wet etching to remove the mask layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Re claim 19, as applied to claim 12 above, Huang et al. disclose all the claimed limitation including the limitation using etch back (see Fig. 3G) to remove the part of the insulation layer (see Figs. 3A-3I; Col. 7, line 16 – Col. 8, line 45).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US/6,413,818) in view of Prall (US/5,387,534).

Re claim 5, as applied to claim 4 in Paragraph 9 above, Hung et al. disclose all the claimed limitation. However, Hung et al. do not specifically disclose the using The method TEOS (tetra-ethyl-oxy-silicate) and ozone to from the insulation layer.

Prall discloses a method of fabrication of a flash memory the method comprises formation of insulation layer (70) using TEOS and ozone in order to provide isolation region between devices (see Figs. 9 and 10; Col. 5, lines 34-41).

Both Huang et al. '818 and Prall '534 teachings are directed to method of fabricating of flash memory cell device the method includes depositing of an oxide isolation between the floating gates. Therefore, the teachings of Huang et al. '818 and Prall '534 are analogous.

Hence, one of ordinary skill in the art would have been motivated to use TEOS and ozone in order to deposit an oxide layer that can provide an isolation region between devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. reference with using of TEOS and ozone during formation insulation layer as taught by Prall in order to deposit of an oxide isolation layer that provides isolation between the device regions.

Re claim 15, as applied to claim 14 in Paragraph 9 above, Hung et al. disclose all the claimed limitation. However, Hung et al. do not specifically disclose the using The method TEOS (tetra-ethyl-oxy-silicate) and ozone to from the insulation layer.

Prall discloses a method of fabrication of a flash memory the method comprises formation of insulation layer (70) using TEOS and ozone in order to provide isolation region between devices (see Figs. 9 and 10; Col. 5, lines 34-41).

Both Huang et al. '818 and Prall '534 teachings are directed to method of fabricating of flash memory cell device the method includes depositing of an oxide isolation between the floating gates. Therefore, the teachings of Huang et al. '818 and Prall '534 are analogous.

Hence, one of ordinary skill in the art would have been motivated to use TEOS and ozone in order to deposit an oxide layer that can provide an isolation region between devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. reference with using of TEOS and ozone during formation insulation layer as taught by Prall in order to deposit of an oxide isolation layer that provides isolation between the device regions.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US/6,413,818) in view of Hsue et al. (US/5,516,713).

Re claim 10, as applied to claim 4 in Paragraph 9 above, Hung et al. disclose all the claimed limitation including removing of the silicon nitride mask layer. However, Hung et al. don not specifically disclose using phosphoric acid as etchant during removal of silicon nitride the mask layer.

Hsue at al. disclose method of fabrication flash memory the method includes depositing of the silicon nitride mask layer (16) and removing of the silicon nitride mask layer using phosphoric acid in order to expose the underlying layer (14) (see Col. 3, lines 13-16).

Both Huang et al. '818 and Hsue et al. '713 teachings are directed to method of fabricating of flash memory cell device the method includes depositing silicon nitride mask layer and removing of the silicon nitride mask layer in order to expose the underlying layer. Therefore, the teachings of Huang et al. '818 and Hsue et al. '713 are analogous.

Hence, one of ordinary skill in the art would have been motivated to use TEOS and ozone in order to deposit an oxide layer that can provide an isolation region between devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. reference with use phosphoric acid during etching of the silicon nitride layer as taught by Hsue et al. in order to expose the underlying layer.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Hara et al. (US/2003/0071297), Yoon (US/6,670,239), and Fujio et al. (US/6,724,035) also disclose similar inventive subject matter.

Correspondence

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823
Brook Kebede

BK
September 22, 2004